ABSTRACT

A semiconductor package includes a chip carrier to receive a semiconductor with a dimension generally greater than 26 mm. The chip carrier has a first coefficient of thermal expansion that is larger than the coefficient of thermal expansion of the semiconductor. A stress inhibiting intermediate mounting substrate is connected to the chip carrier through a first array of solder connections. The stress inhibiting intermediate mounting substrate has a second coefficient of thermal expansion that is larger than the coefficient of thermal expansion of the chip carrier and smaller than or equal to the coefficient of thermal expansion of the printed circuit board. Alternate preferred inventive embodiments allow for the cleaning and removal of residual flux and other debris in packaging.